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MS-7404

Version 1.3

CPU	Generation	DUAL CORE	FSB	L2 Cache	HT	EM64T	EIST	VT
Core 2 Dual	Conroe(TBD series)	V	1066/800	2 x 4MB	X	V	V	V
	PD Extreme Edition	V	800	2 x 1MB	V	V	V	V
Pentium D	Presler (9 series)	V	800	2 x 2MB	X	V	V	V
	Smithfield (8 series)	V	800	2 x 1MB	X	V	>=830	X
Pentium 4	P4 Extreme Edition	X	1066	2MB	V	V	V	X
	Cedar Mill (6 series)	X	800	2MB	V	V	V	"2" in last code
	Prescott (5 series)	X	533/800	1MB	V	"1" in last code	X	X
Celeron D	Cedar Mill (TBD series)	X	TBD	512KB	X	V	X	X
	Prescott (3 series)	X	533	256KB	X	X	X	X

System Chipset:

Intel Bearlake G31- GMCH (North Bridge)

Intel ICH7

On Board Chipset:

BIOS -- FWH 4Mb

AC97 AUDIO -- ALC888

LPC Super I/O -- W83627DHG

LAN -- Realtek RTL8111B

CLOCK -- ICS9LPR502

Main Memory:

2 CHANNEL DDR II * 1 (Max 4GB)


Expansion Slots:

miniPCIE x1

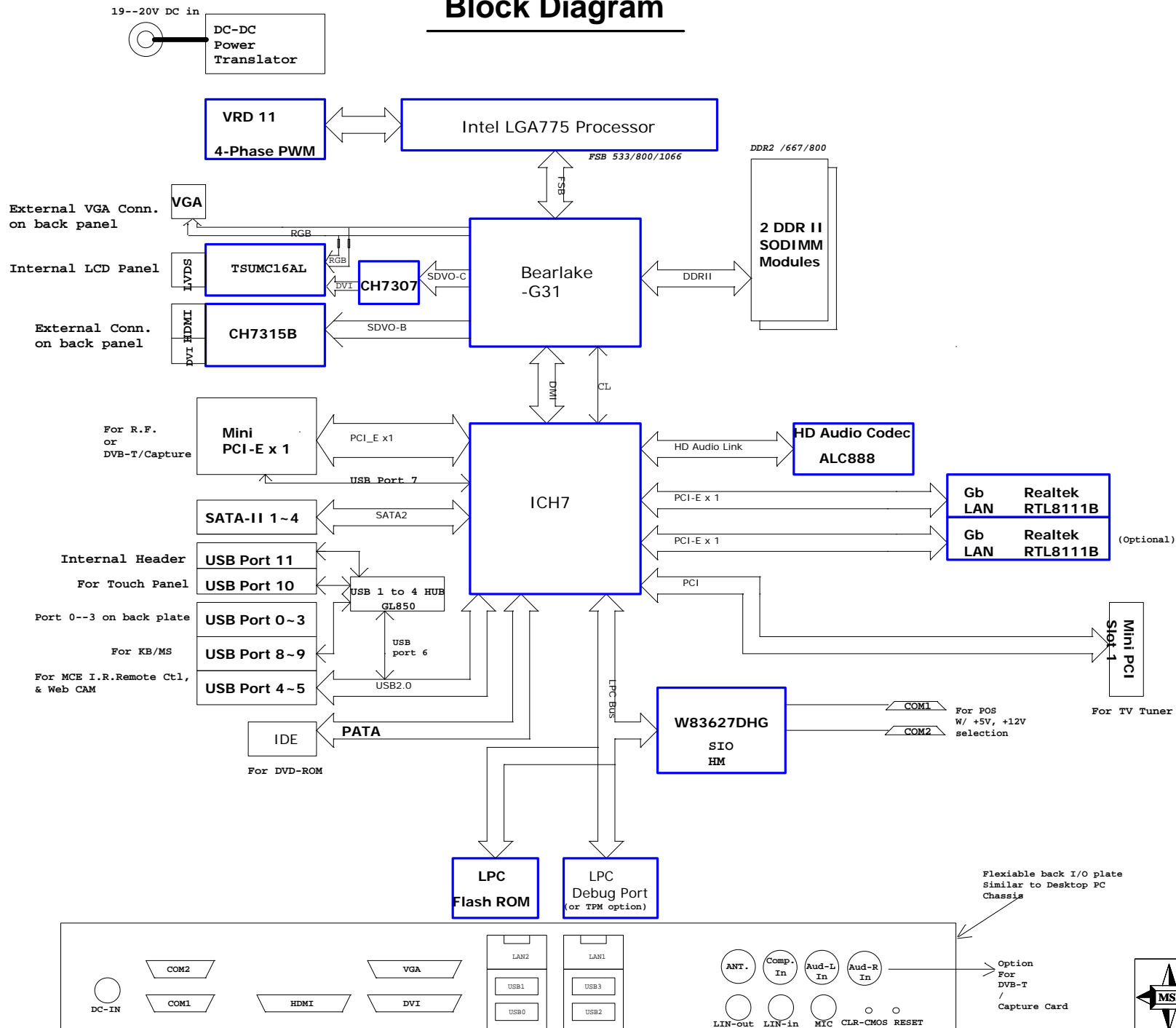
mini PCI SLOT * 1

Intersil PWM:

Controller: VRD11 Intersil 6326 4Phase

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Block Diagram

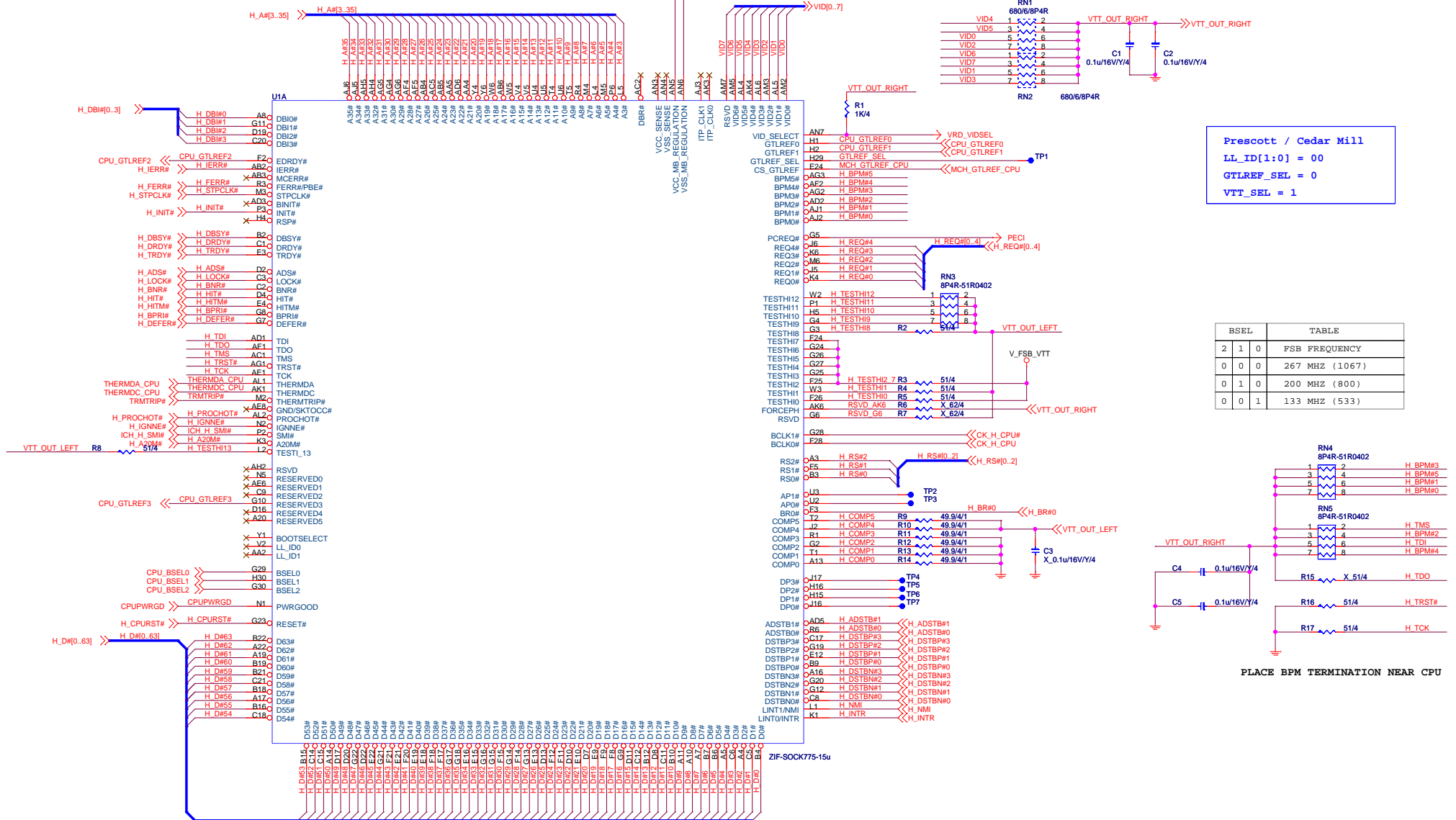


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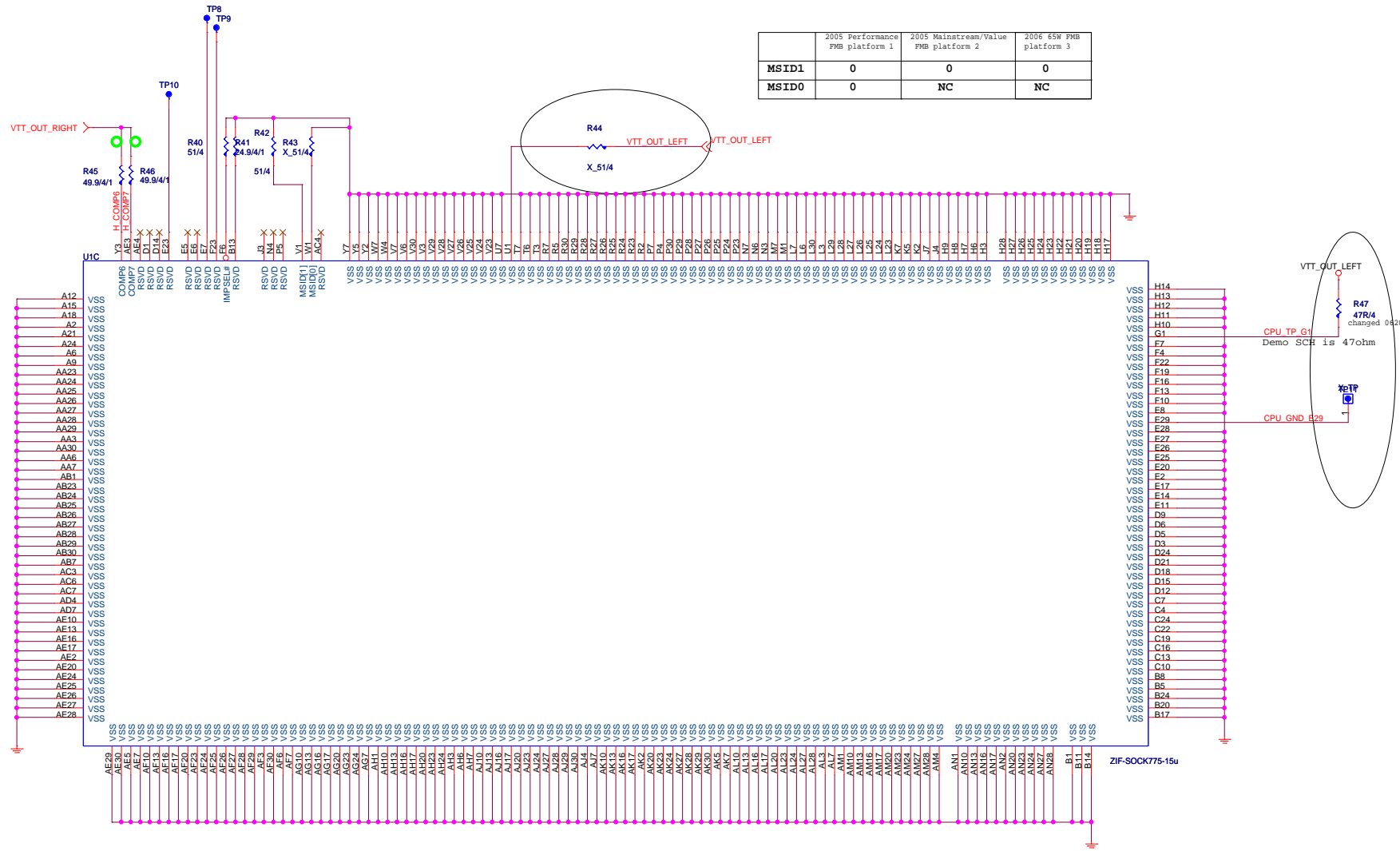
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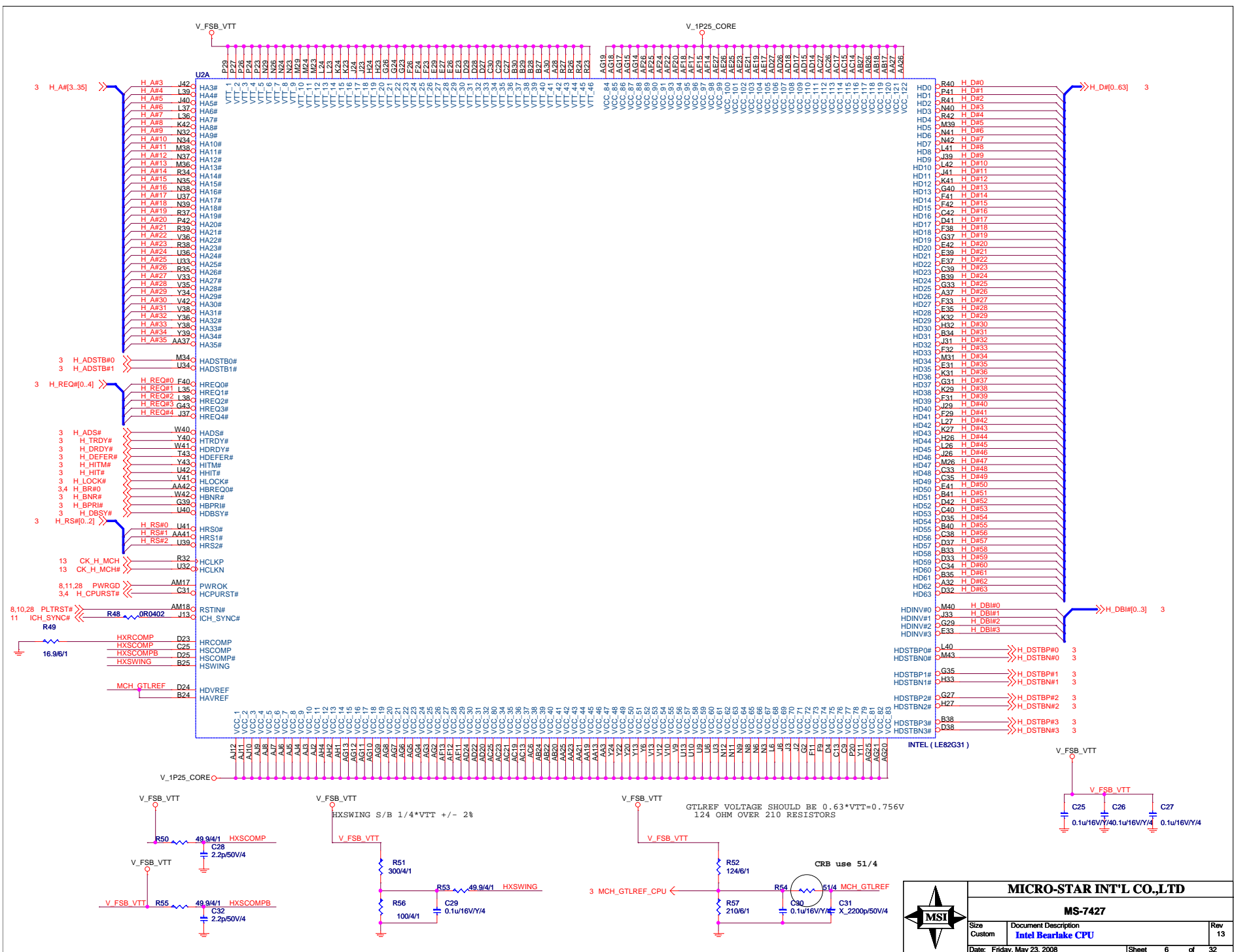
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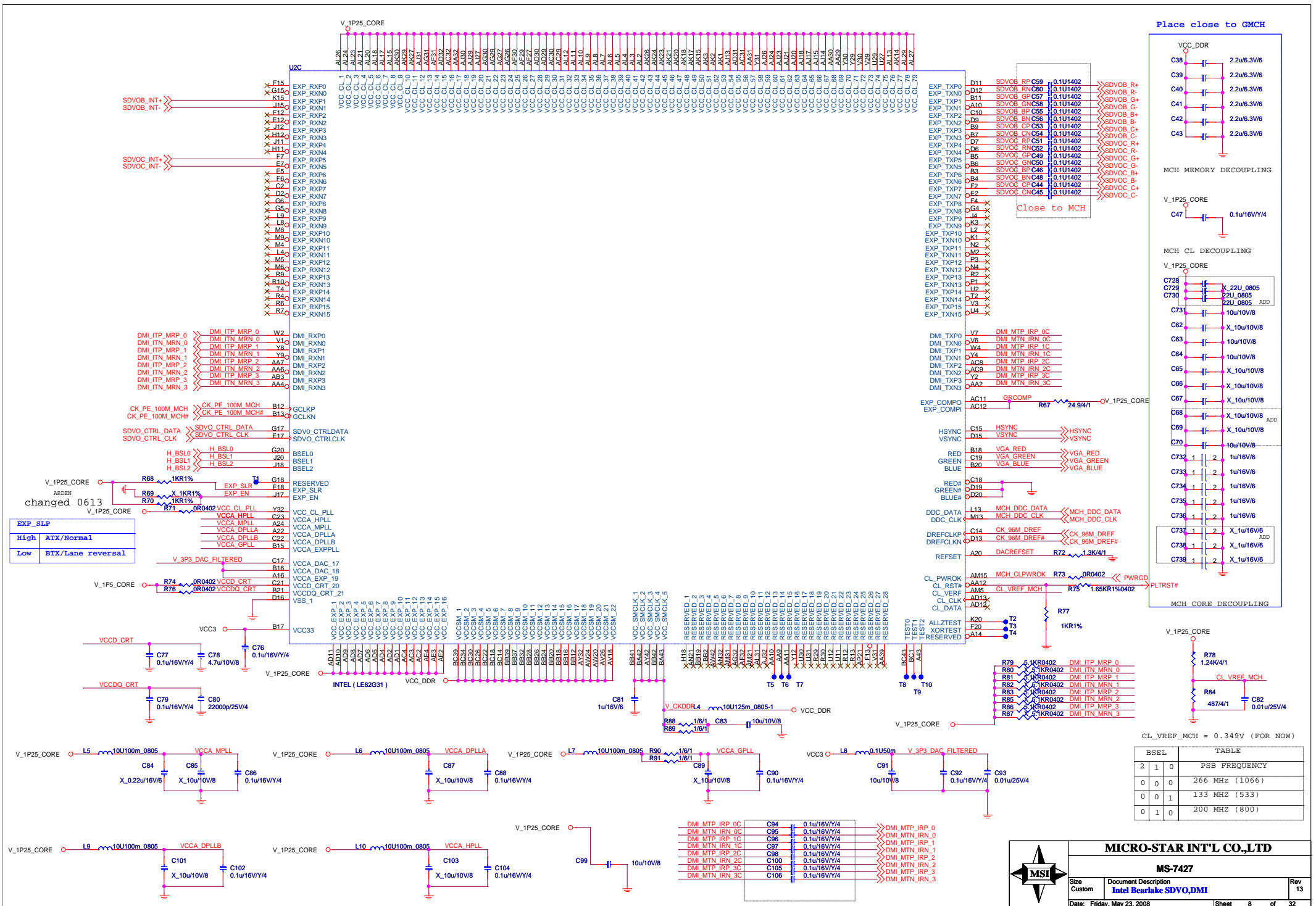
CPU SIGNAL BLOCK

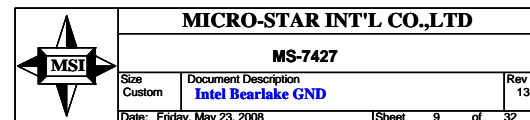


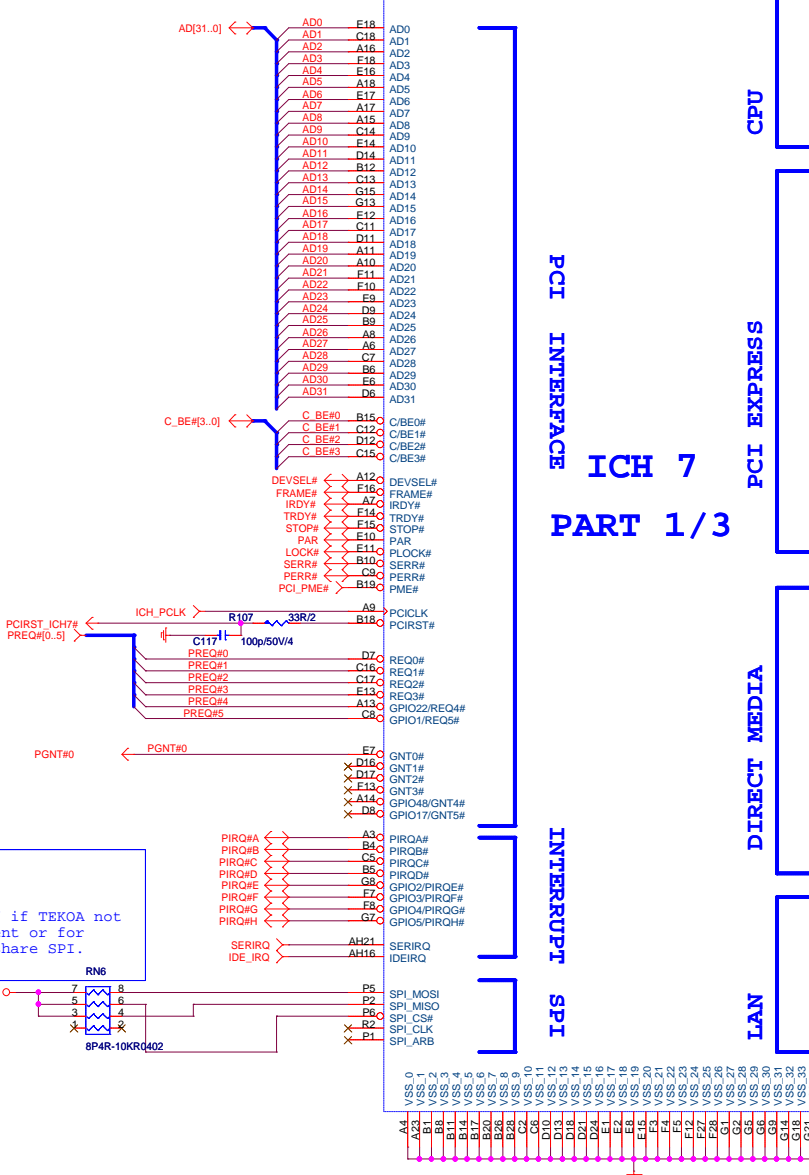
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MSID1	0	0	0
MSID0	0	NC	NC





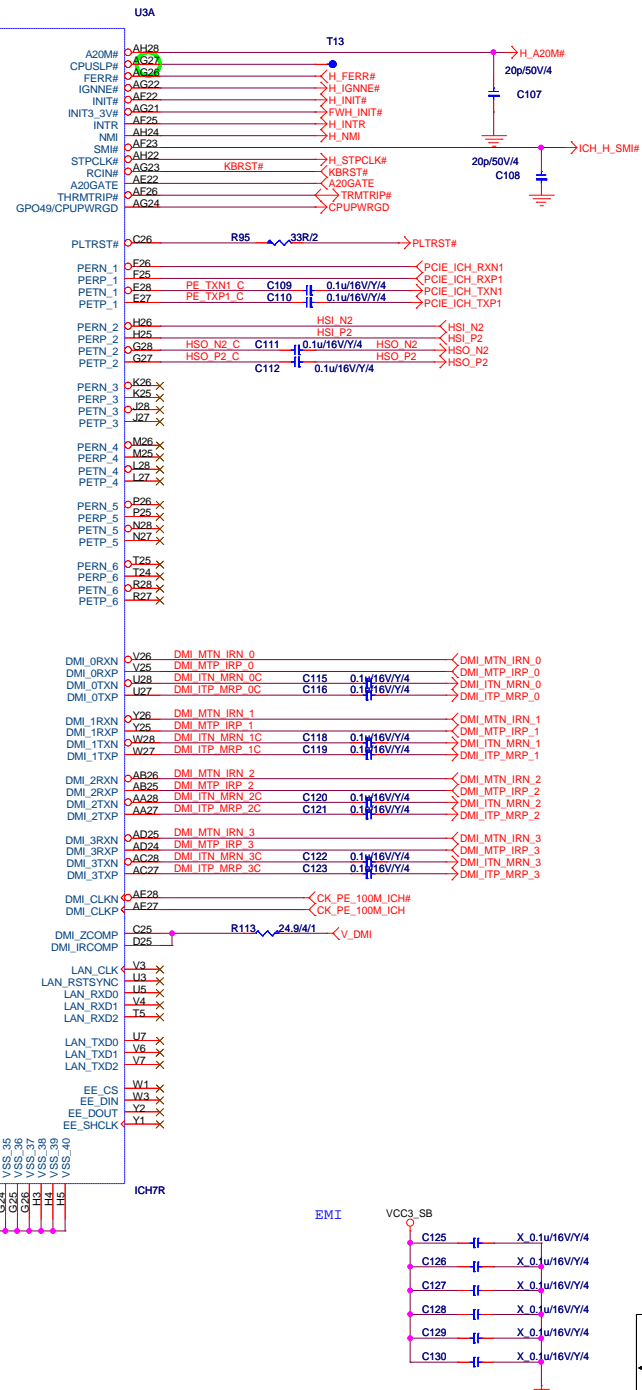


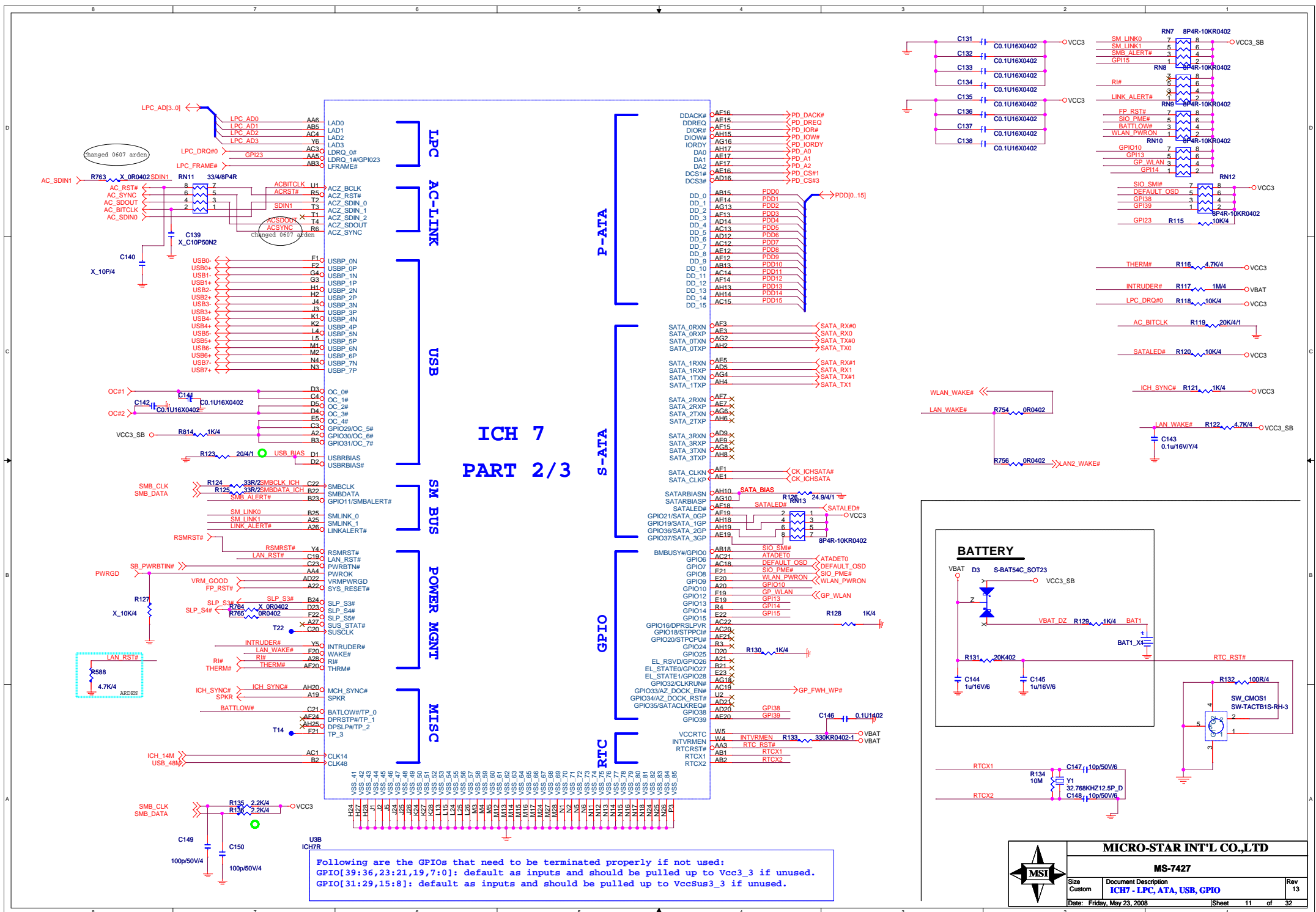




ICH 7
PART 1/3

Stuff if TEKOA not present or for Non-share SPI.





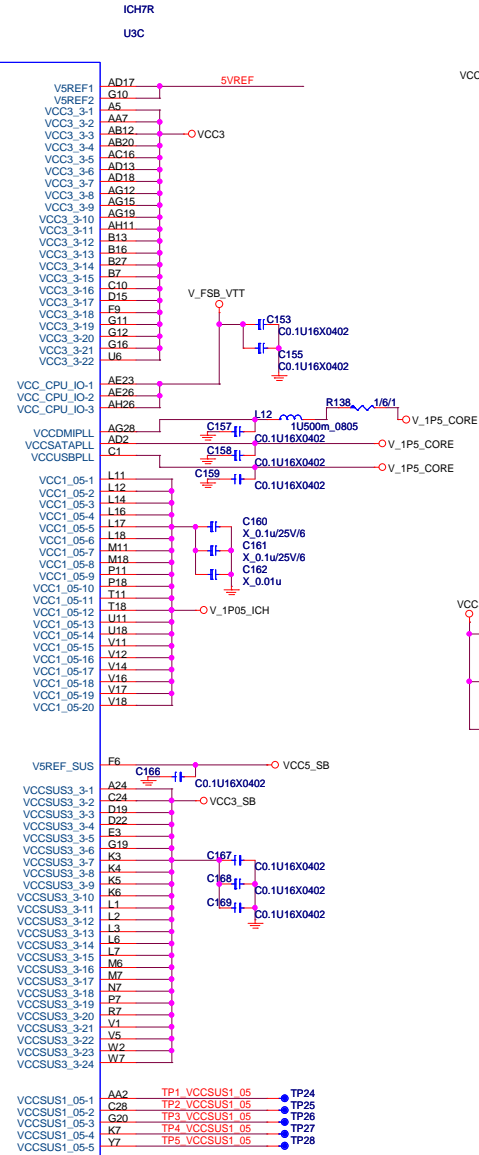
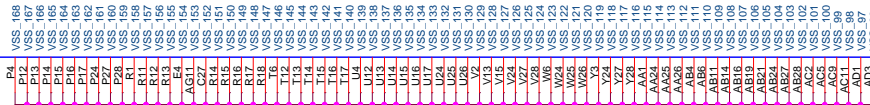
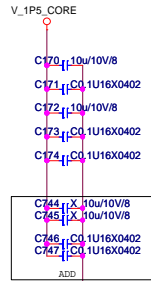
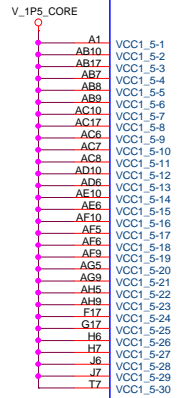
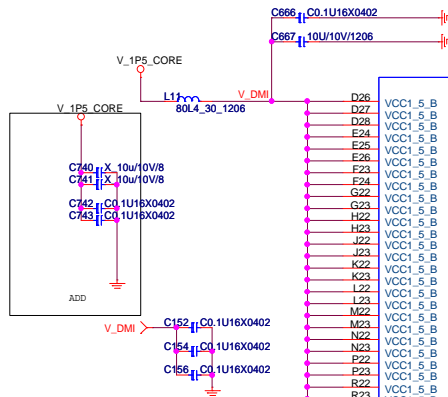
ICH 7
PART 3/3

1.5V DMI POWER

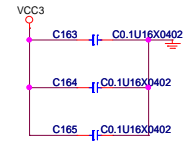
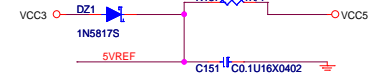
S0 POWER

S5 POWER

1.5V CORE WELL POWER



5VREF Sequencing Circuit

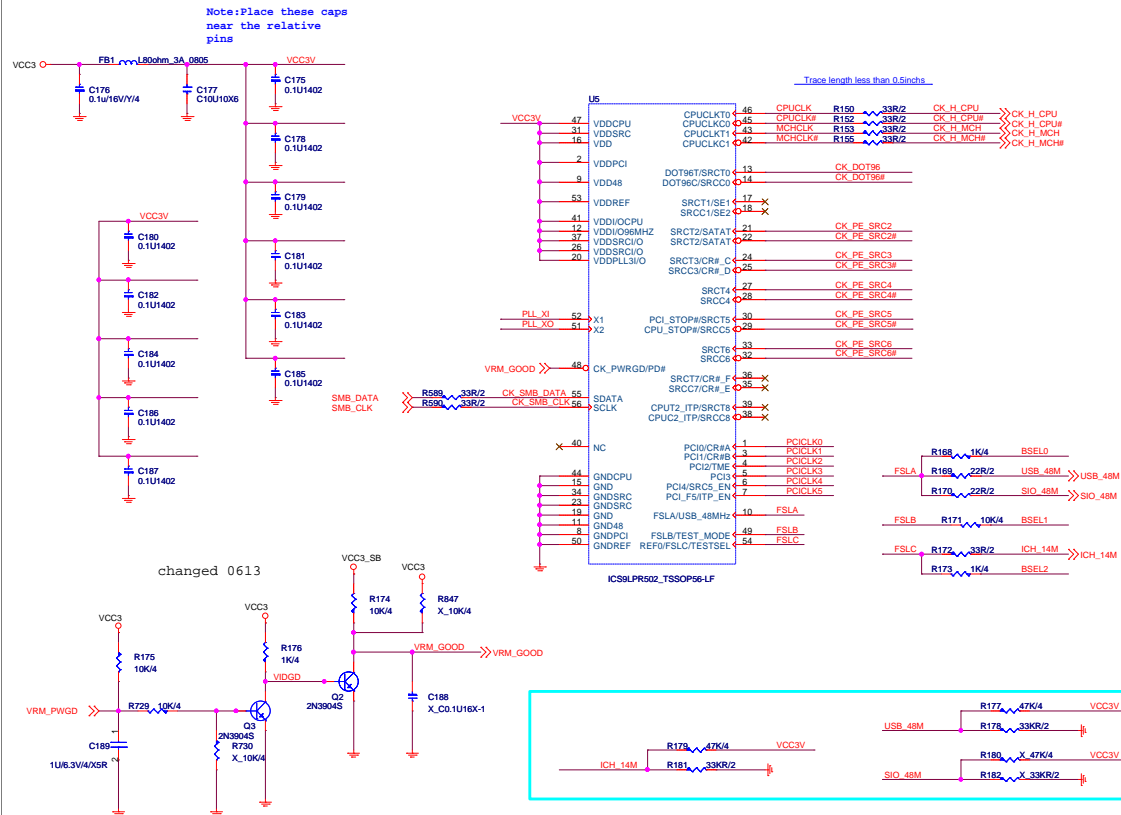


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Clock Generator - ICS9LPR502



CK PE SRC2# R139 33R/2 CK ICHSATA# CK ICHSATA#
 CK PE SRC2 R140 33R/2 CK ICHSATA# CK ICHSATA#
 CK PE SRC3# R141 33R/2 CK PE 100M ICH# CK PE 100M MCH#
 CK PE SRC3 R142 33R/2 CK PE 100M ICH# CK PE 100M MCH#

CK PE SRC5# R145 33R/2 CK PE 100M WLAN# CK PE 100M WLAN#
 CK PE SRC5 R146 33R/2 CK PE 100M WLAN# CK PE 100M WLAN#

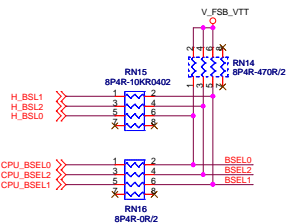
CK DOT96# R147 33R/2 CK 96M DREF# CK 96M DREF#
 CK DOT96 R148 33R/2 CK 96M DREF# CK 96M DREF#
 CK PE SRC4# R149 33R/2 CK PE 100M ICH# CK PE 100M ICH#
 CK PE SRC4 R151 33R/2 CK PE 100M ICH# CK PE 100M ICH#
 CK PE SRC5 R154 33R/2 CK PE 100M LAN2 CK PE 100M LAN2#
 CK PE SRC5# R155 33R/2 CK PE 100M LAN2 CK PE 100M LAN2#
 PCCLK1 R157 33R/2 FWH_PCLK FWH_PCLK
 PCCLK2 R158 33R/2 LPC_DBG_PCLK LPC_DBG_PCLK
 PCCLK3 R159 33R/2 ICH_PCLK ICH_PCLK
 PCCLK3 R160 33R/2 PCI_CLK0 PCI_33M_SLOT
 PCCLK0 R161 33R/2 SIO_PCLK SIO_PCLK

Changed 0607 arden

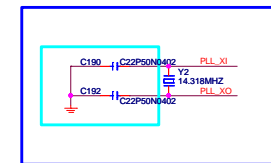
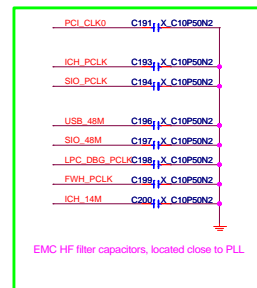
PCCLK4 R164 10K/4 R165 X 10K/4
 0 = PCI_STOP#/CPU_STOP#
 1 = SRC5/SRC5#

PCCLK2 R166 X 10K/4 R167 10K/4
 0 = Overclocking of CPU and SRC Allowed
 1 = Overclocking of CPU and SRC NOT allowed

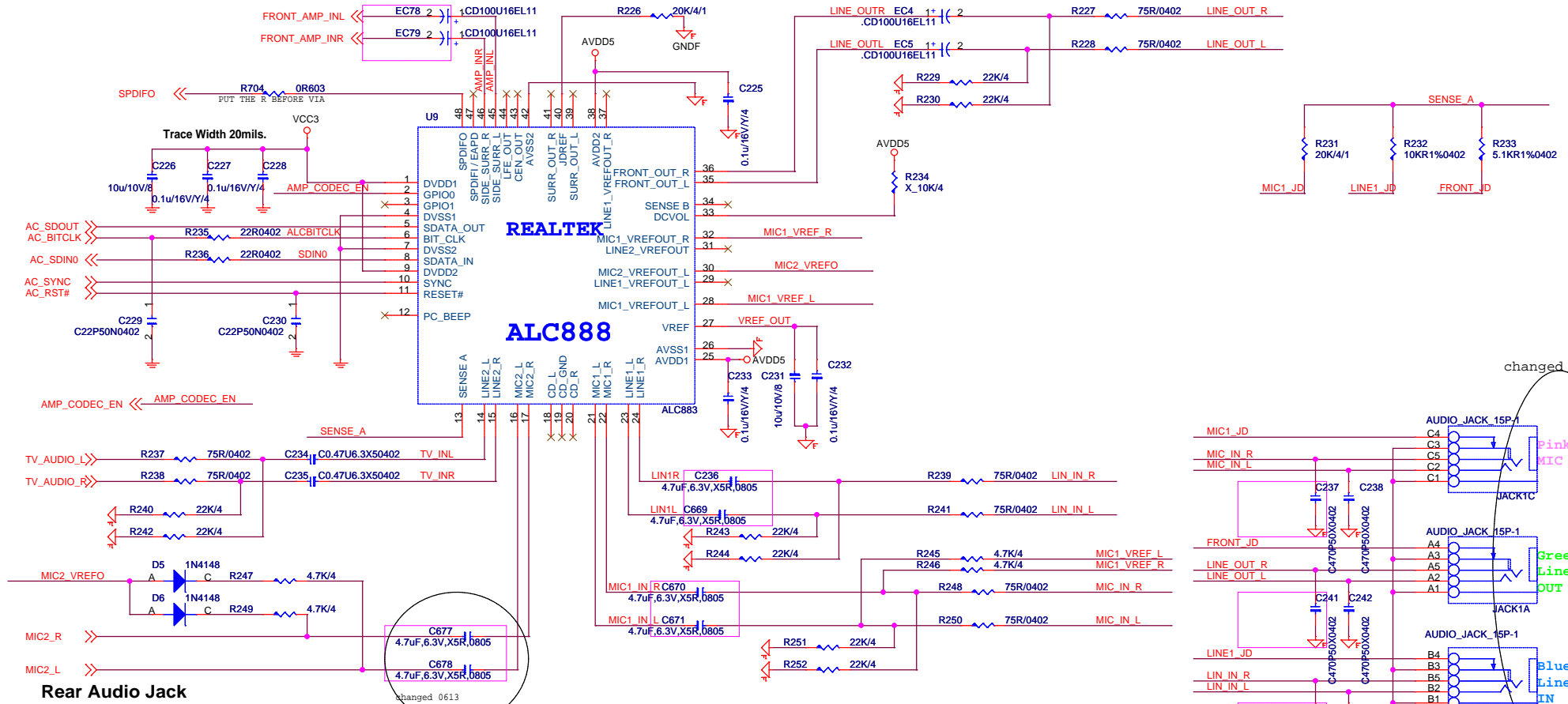
BSEL[0..2] Level Shift



BSEL	TABLE
0 0 0	266 MHz (1066)
0 0 1	133 MHz (533)
0 1 0	200 MHz (800)

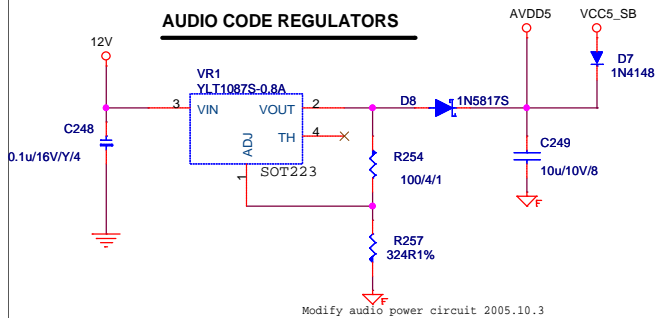


Realtek ALC888 CODEC

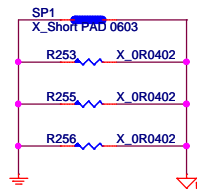


Rear Audio Jack

AUDIO CODE REGULATORS

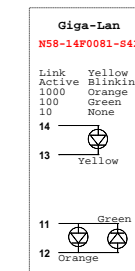
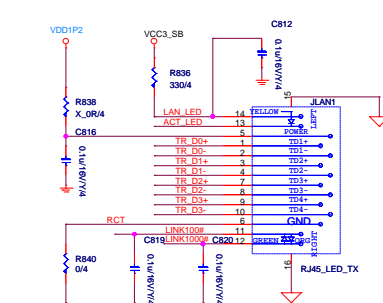
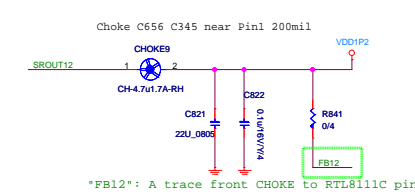
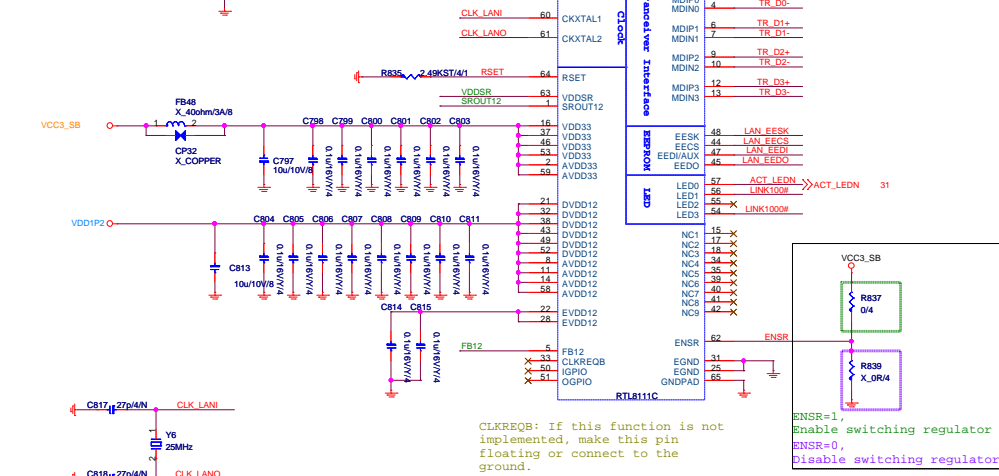
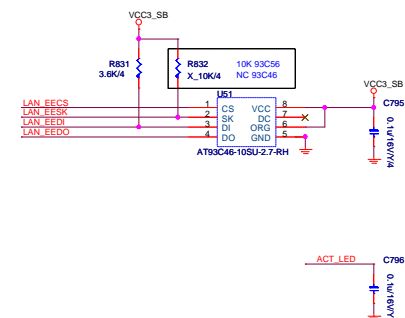
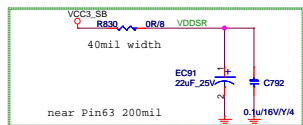


EMI Solution



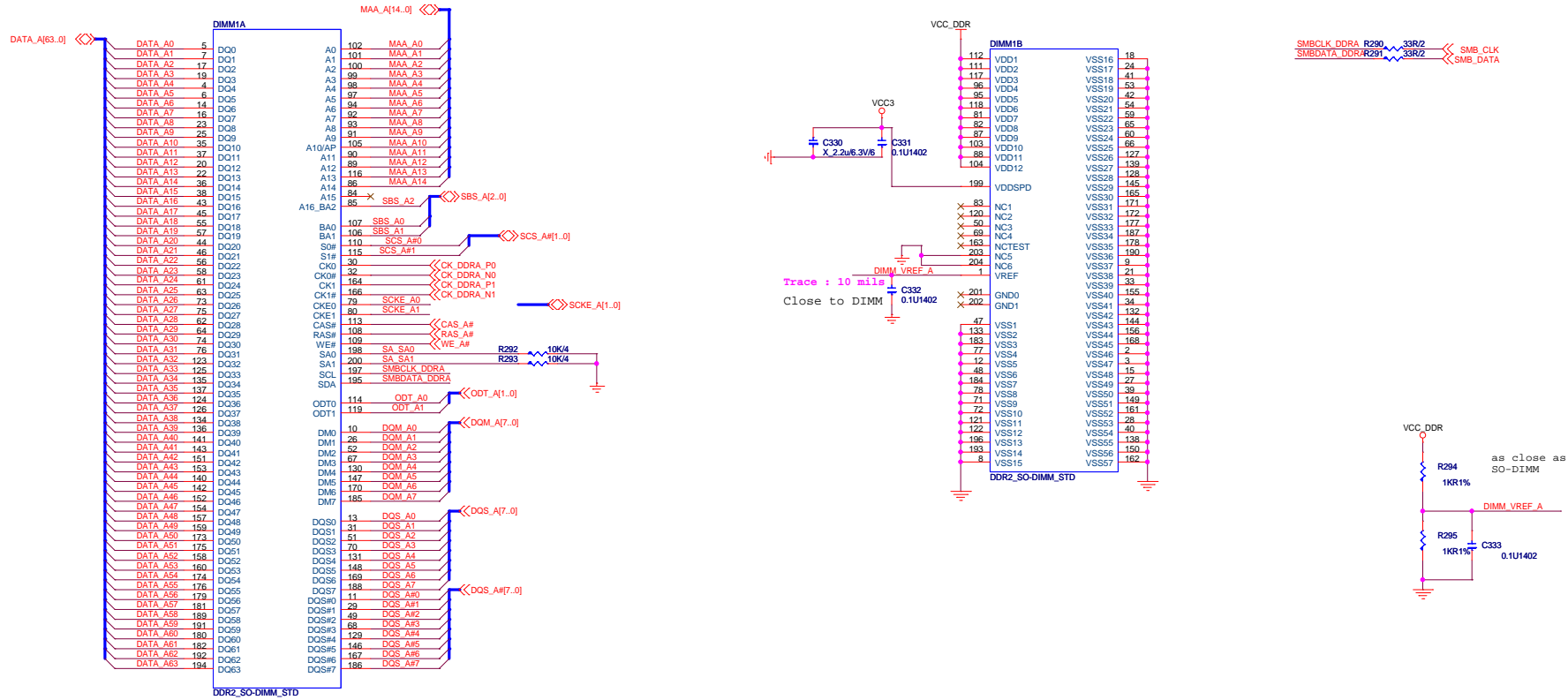
Add R227 according to EMI suggestion
2006.9.28

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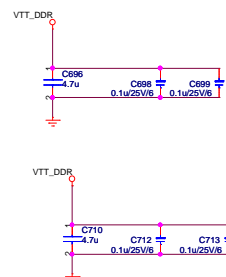
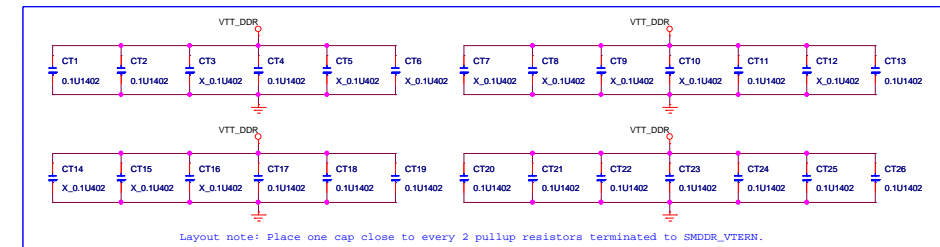
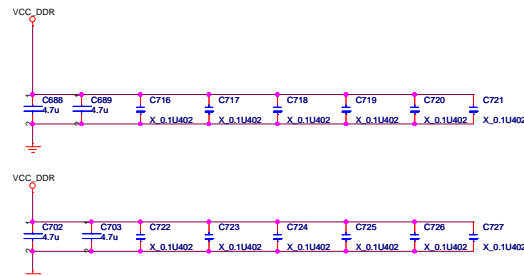


DDR2 SODIMM A0

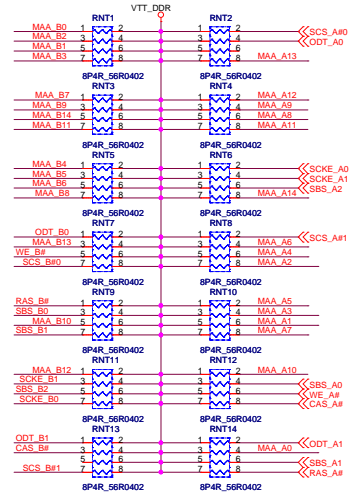
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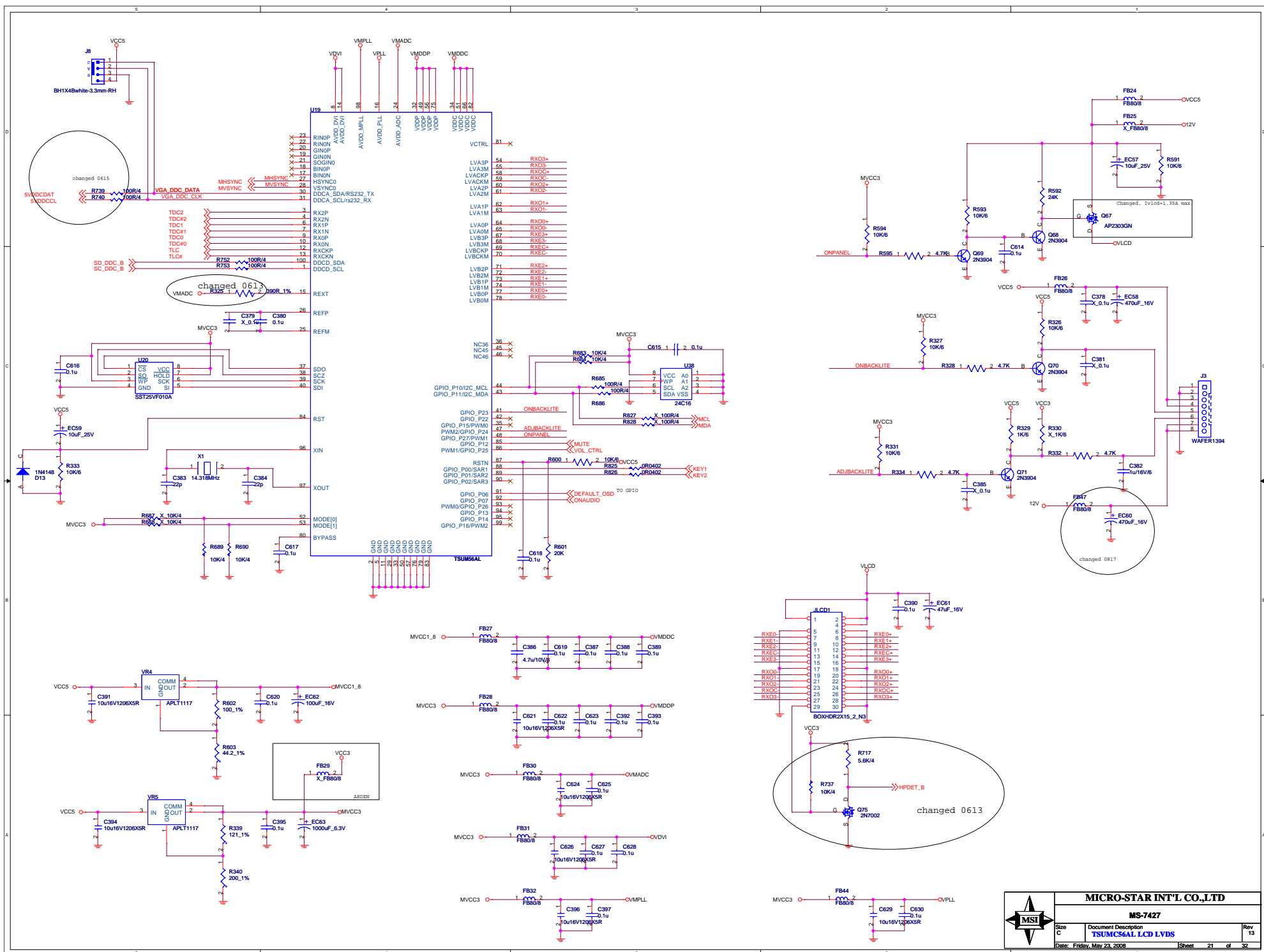


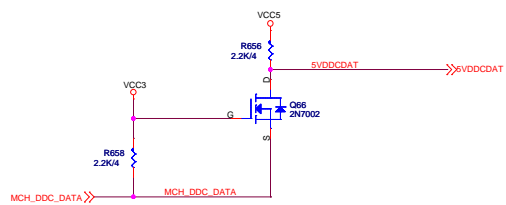
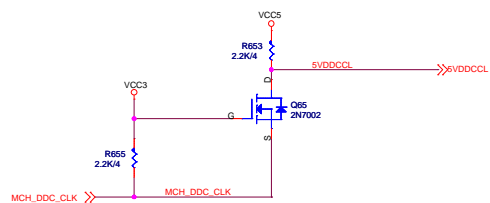
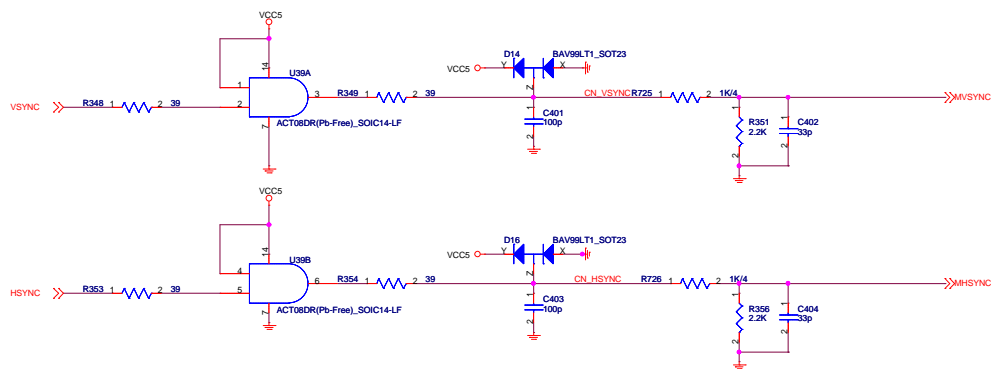
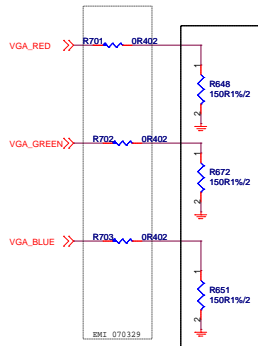
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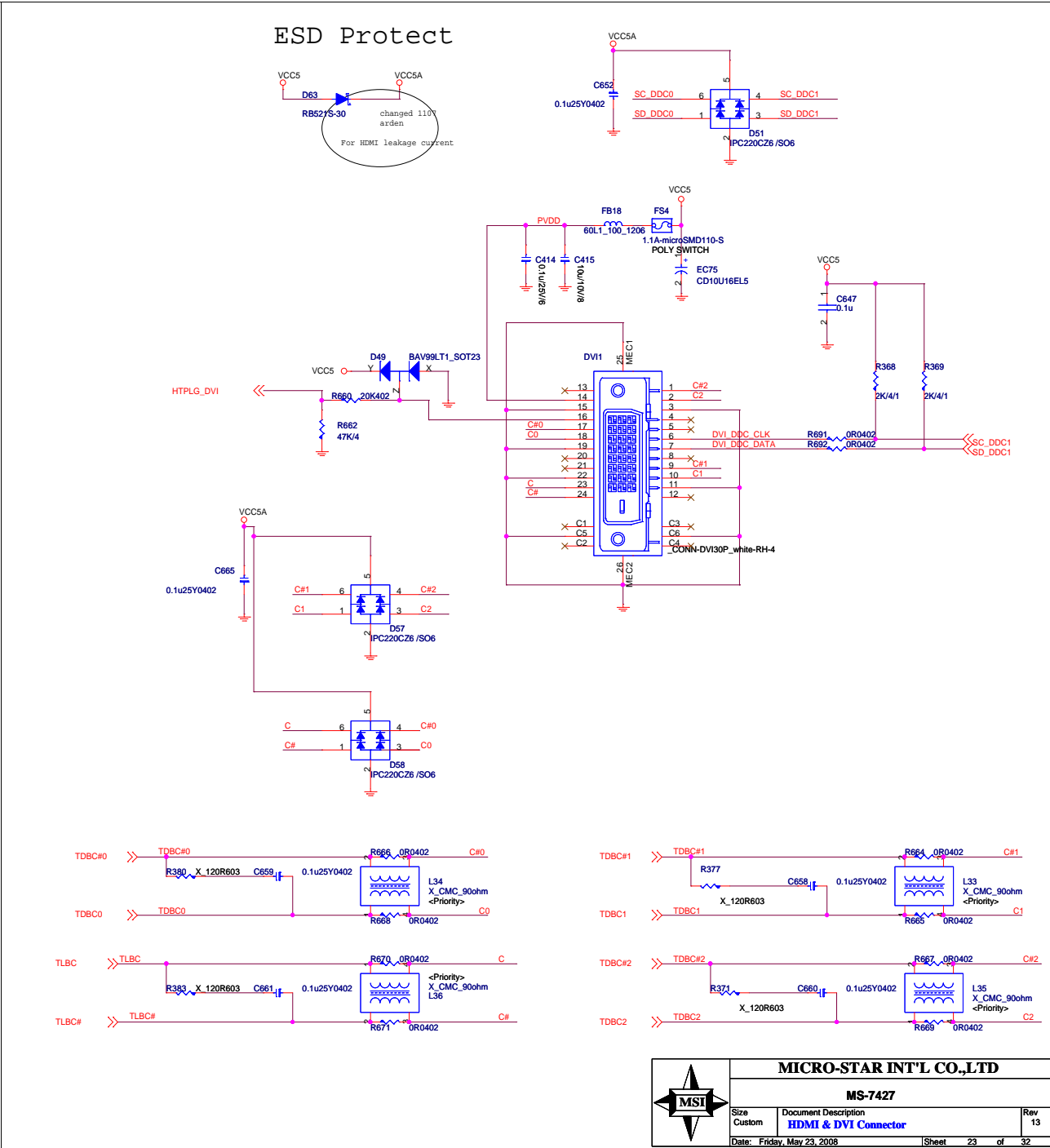
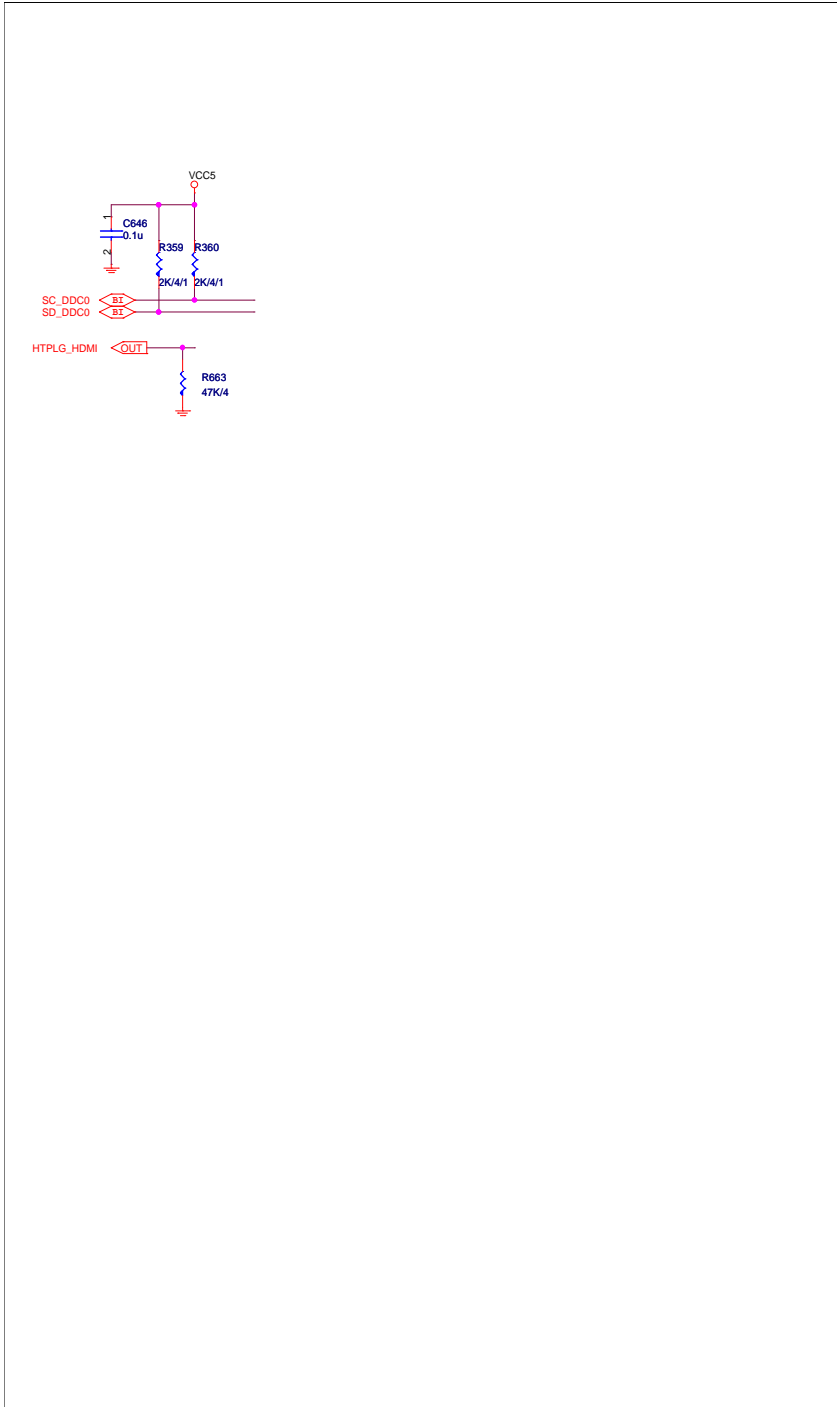


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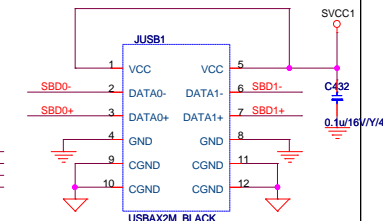
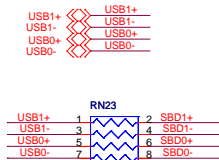
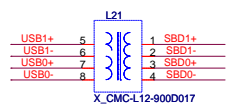
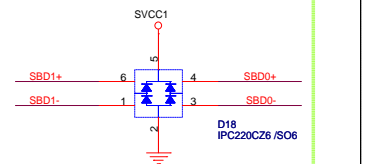
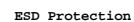
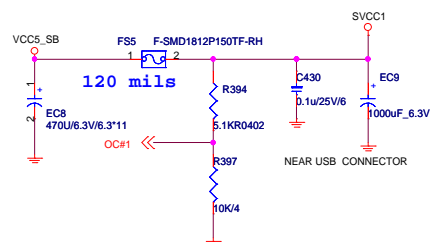




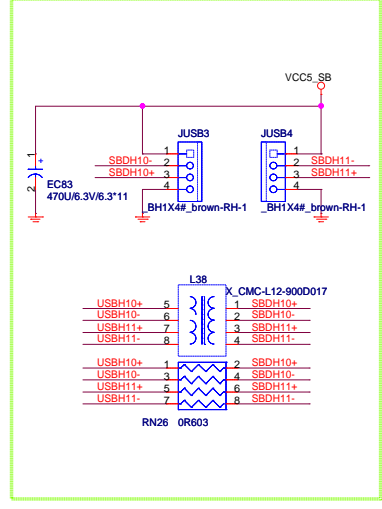
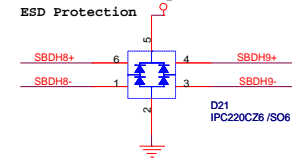
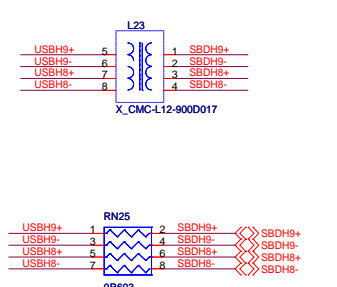
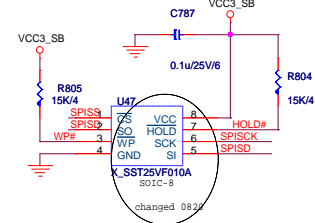
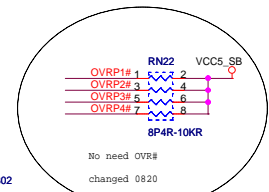
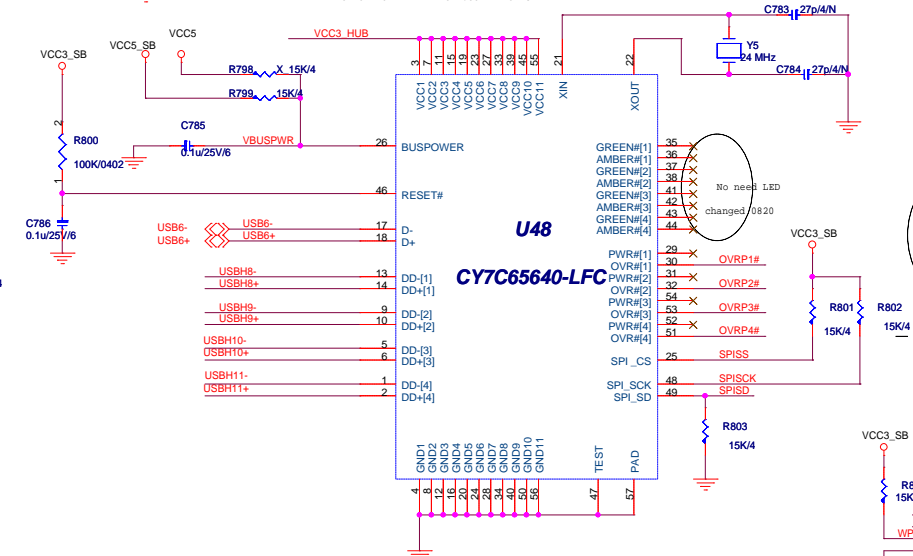
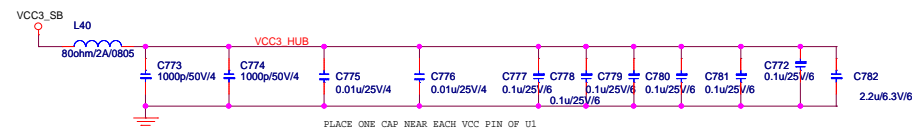
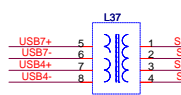
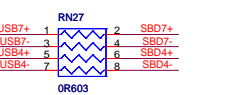
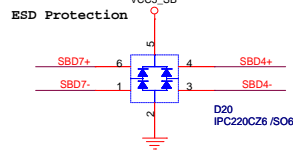
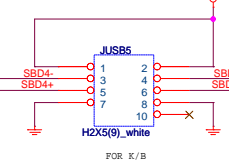
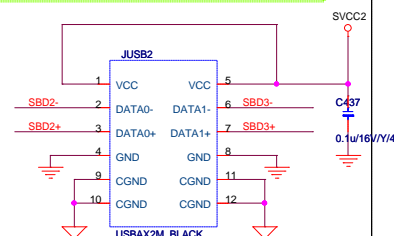
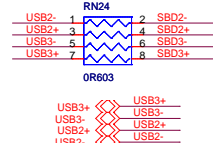
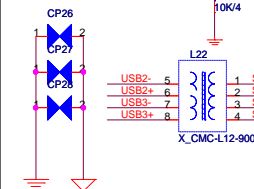
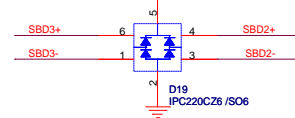
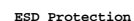
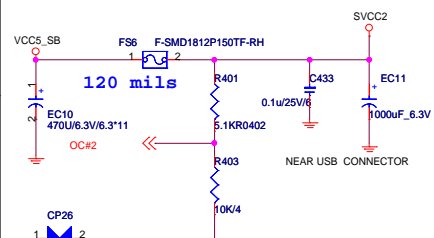




POWER CIRCUIT FOR USB PORT 0 1



POWER CIRCUIT FOR USB PORT 2 3

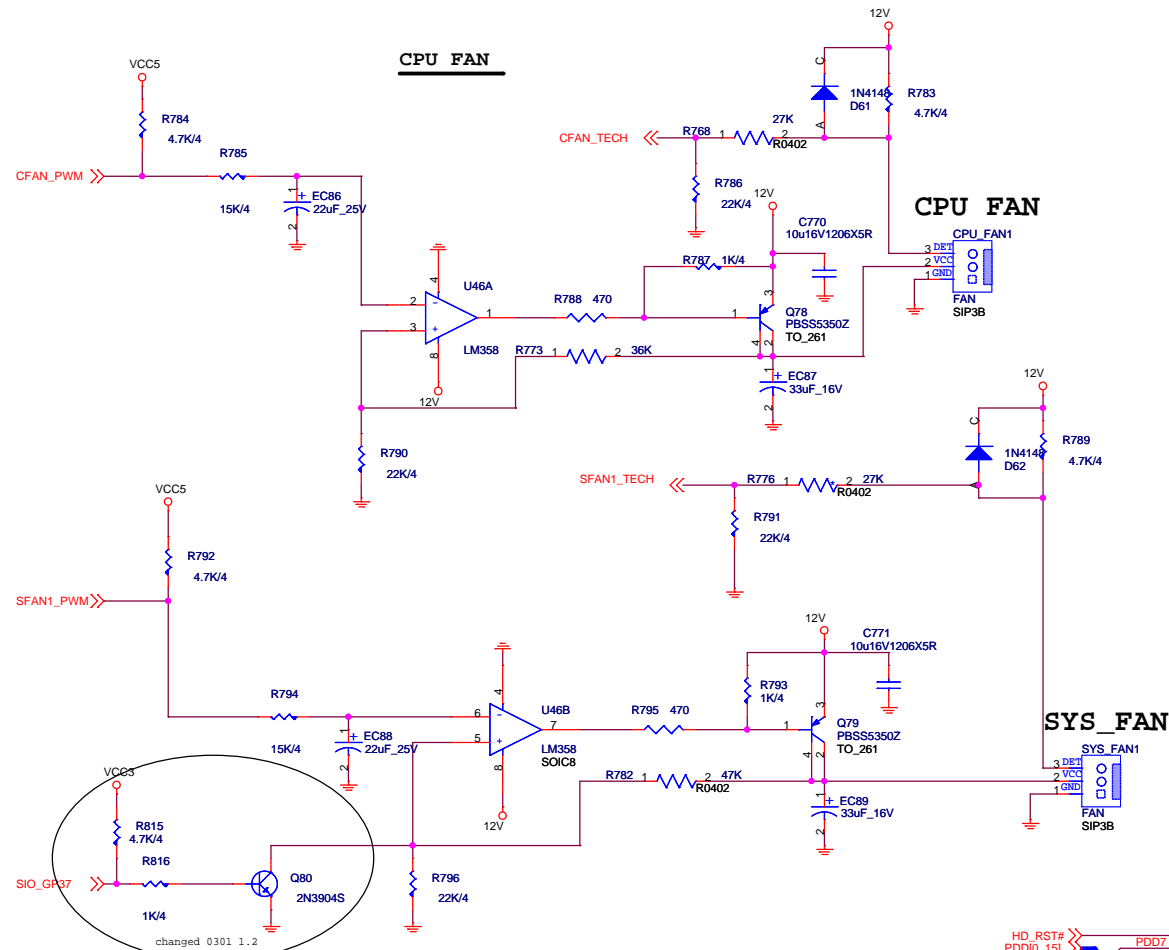


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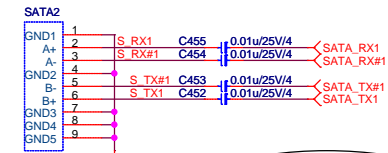
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CPU FAN

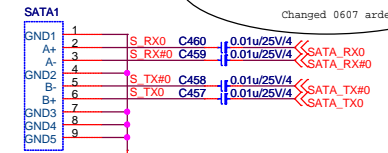


CPU FAN

SYS_FAN



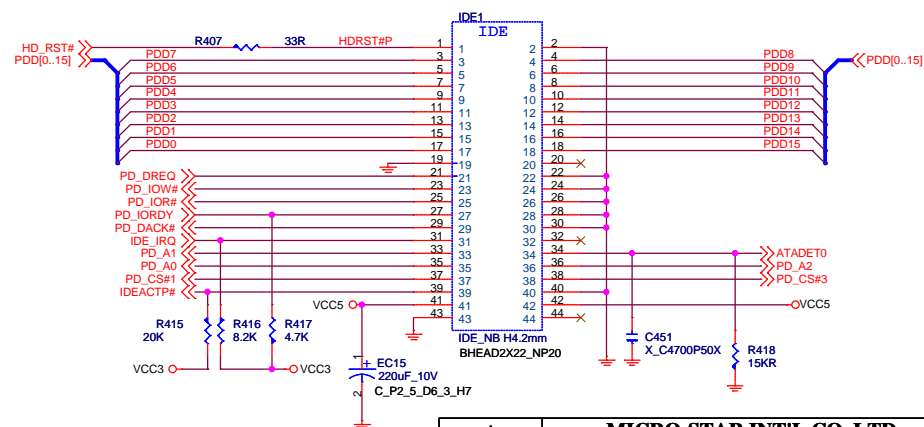
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SATA_RA_CON



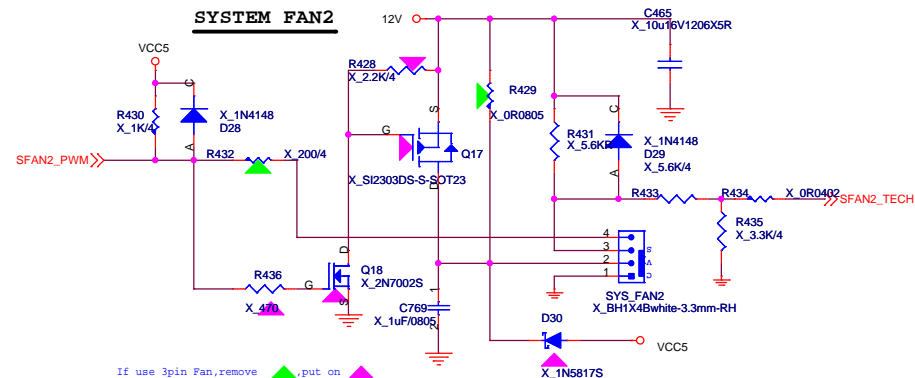
CON_SATA_1X7
SATA_RA_CON

SYSTEM FAN1

ATA 33/66/100 IDE Connectors



SYSTEM FAN2



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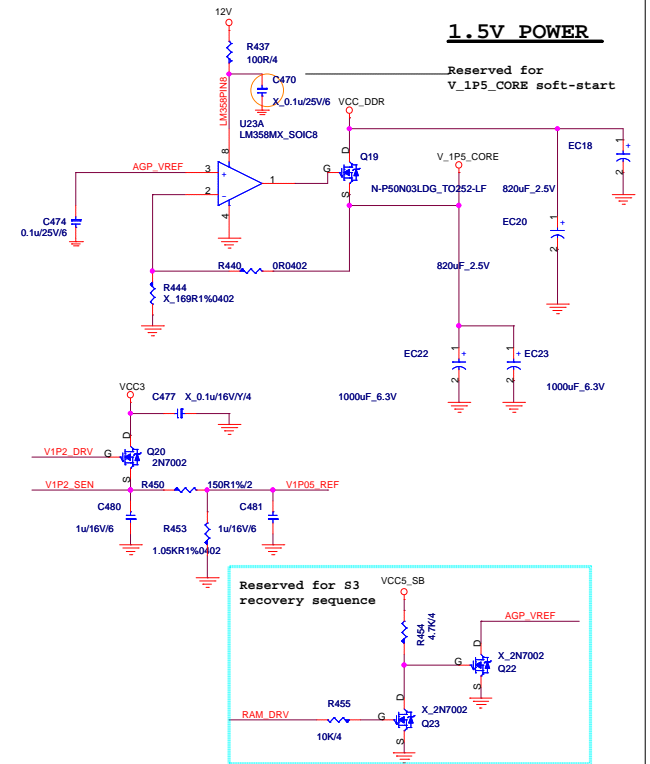
If use 3pin Fan,remove ,put on
If use 4pin Fan,remove ,put on

ACPI Controller MS-7

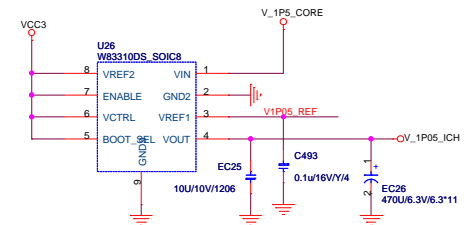


DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

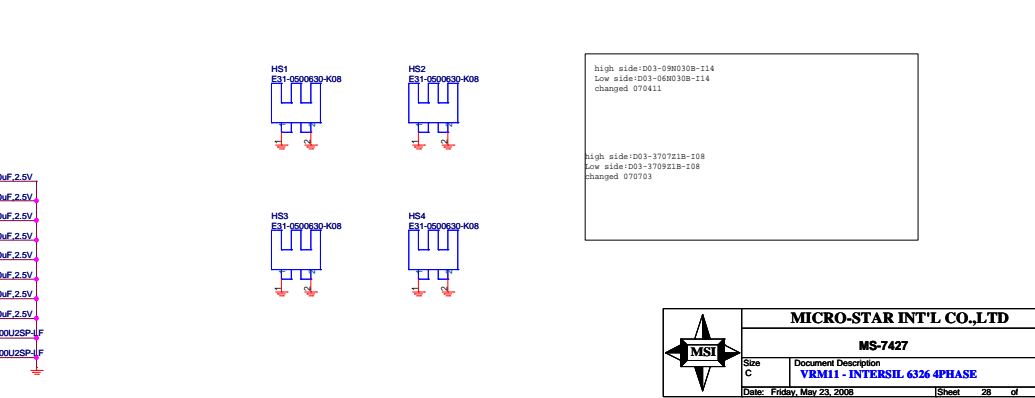
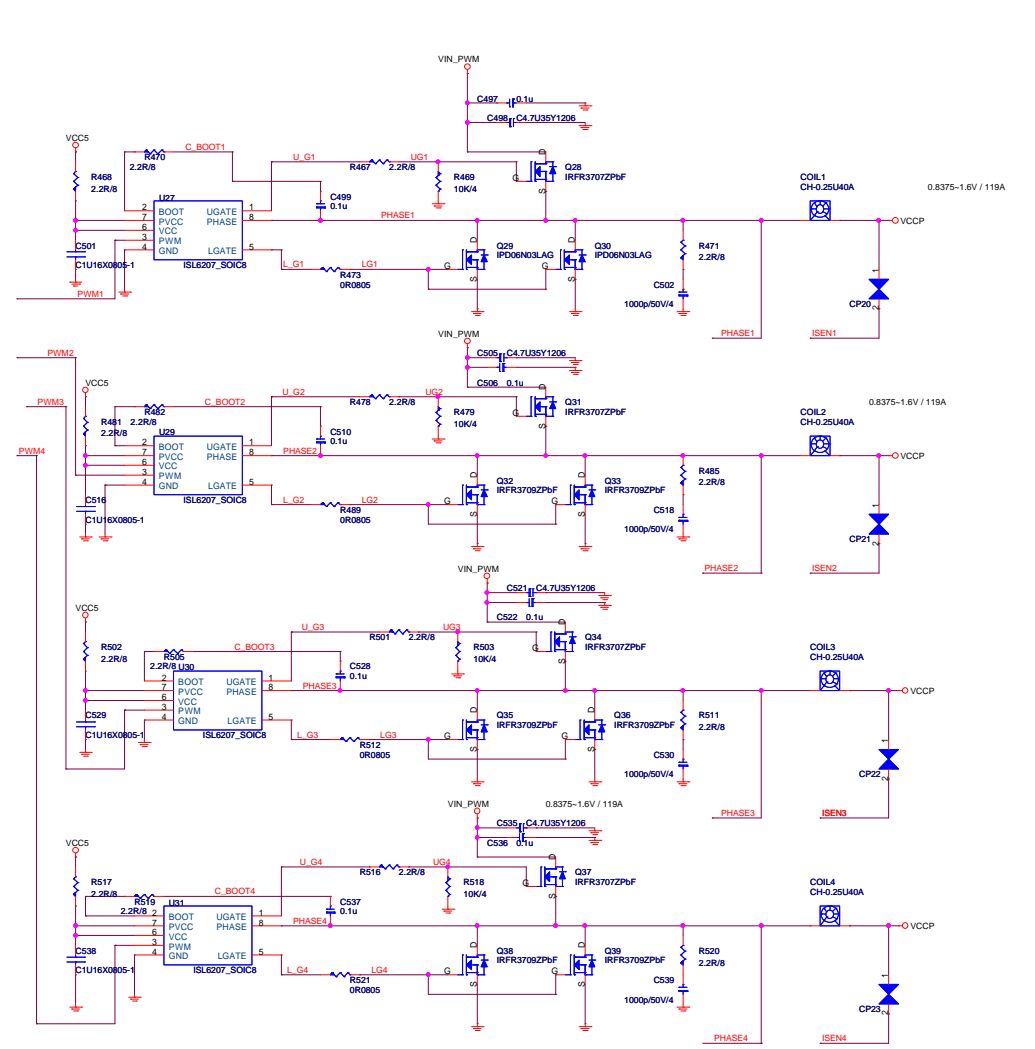
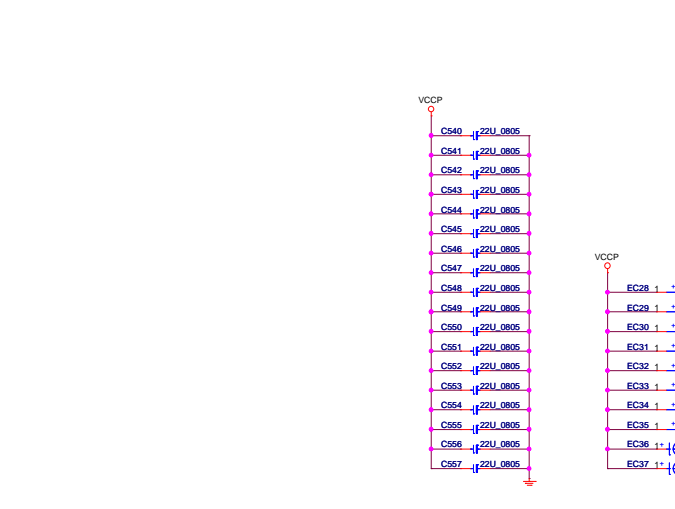
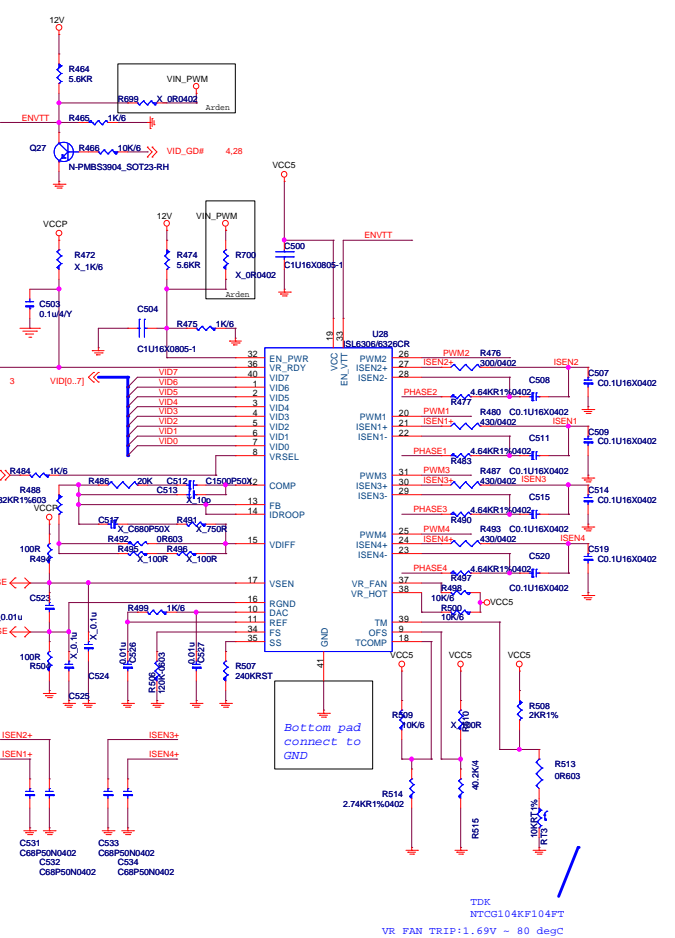
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH



V_1P05 ICH MAX 1.31A

VTT SEL

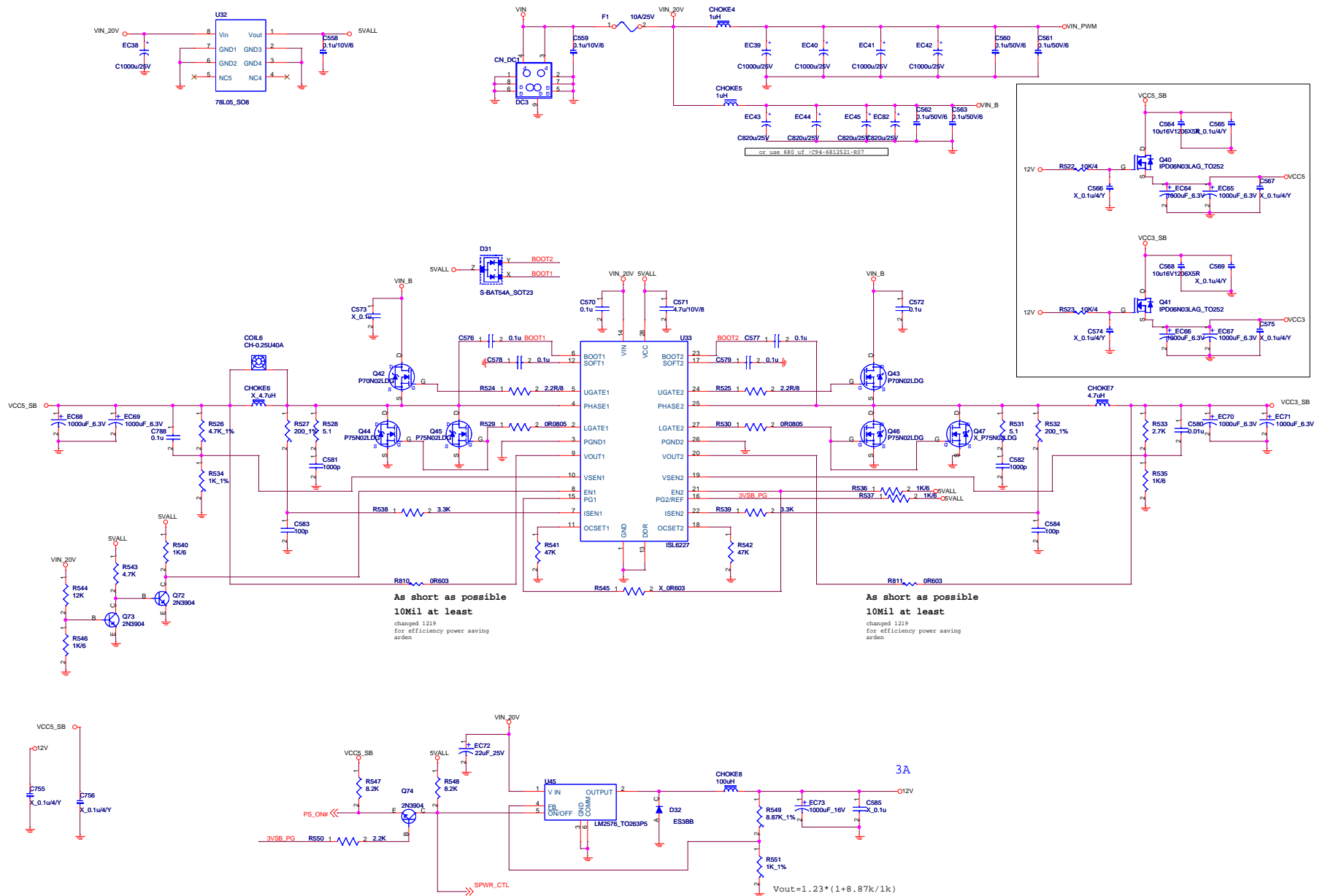
VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.



Modified values:
 1. R488: 2.32k ohm (droop)
 2. R515: 40.2k ohm (offset)
 3. C513: X (comp)
 4. C517: X (comp)
 5. R491: X (comp)
 6. 5.6 reserved.
 changed 0821 by power team

high side: D03-080030B-114
 low side: D03-080030B-114
 changed 070411

high side: D03-370721B-108
 low side: D03-370721B-108
 changed 070703



GMCH 1.25V POWER
(21.3A)

$I_{ocp} * DCR_{max} = I_x * R_{csn}$
 $R_{csn} \geq (40amp * 0.93 m\Omega) / 80uA$
 $\geq 470 \Omega$

Power team fine-tune to eliminate under/over-shoot.

VCC DDR POWER

VCC5_SB 12V

D37 1N5817S

R576 2.2R/8

R577 200K/4

R578 2.2R/8

R579 2K/4/1

R581 2K/4/1

R582 1KR1%0402

R583 34.9KR1%0402

R584 34.9KR1%0402

R585 1.15KR1%0402

R586 22K/4

R587 56K/4/1

C603 1u/16V/6

C605 1u/16V/6

C606 0.1u/16V/Y/4

C610 1u/16V/6

C611 0.1u/16V/6

C607 1u/25V/8

C608 1000p/50V/4

C612 4700p/50V/4

U37

RR VCC12

BOOT UG

5VSB PHASE

PI LG

PVCC GND

SS

RT

I_LIND

GND

MS-11PQV_QFN16-LF

CSP

CSN

FB

COMP

CHOKE2 1uH

EC53 CD1000U16EL20-1

EC54 CD1000U16EL20-1

Q54 N-P603BDG_TO252

Q55 N-P603BDG_TO252-LF

CHOKE3 1uH

CP30

CP31 820uF_2.5V

EC55

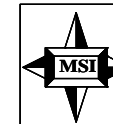
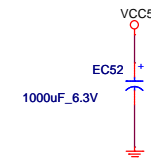
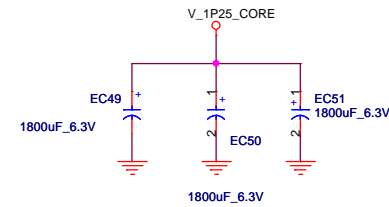
Vout=1.8V 12A

VCC5_SB

RAM_VREF

Power team fine-tune to eliminate under/over-shoot.

RAM_VREF

**MS-7427**

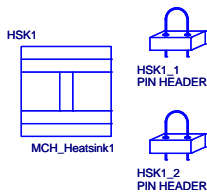
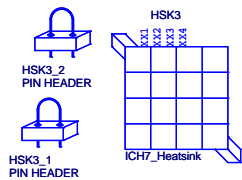
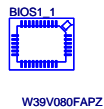
Document Description
DDR&GMCH Power

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Date: Friday, May 23, 2008

Sheet	31	of	32
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MANUAL PART



Inn1



X_PIN1*2
Single-ended 50ohm W=6.5



X_PIN1*2
differential 95ohm W=5.5 S=8



X_PIN1*2
differential 95ohm W=5.5 S=8

Top OR
bottom



X_PIN1*2
Single-ended 50ohm W=7



X_PIN1*2
differential 95ohm W=5.5 S=7

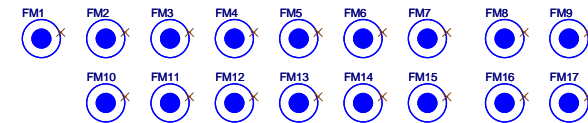


X_PIN1*2
differential 95ohm W=5.5 S=7



X_PIN1*2
Single-ended 30ohm W=9

Optical Fiducial Marks



Mounting Holes

